REMARKS

Applicant respectfully requests reconsideration of this application. Claims 1-27 are pending. Claims 1-3, 5-9, 11-14, 18, 20-24, 26, and 27 have been amended. No claims have been added. No claims have been cancelled.

Therefore, claims 1-27 are now presented for examination.

Claim Rejection under 35 U.S.C. §101

The Examiner rejected claims 22-27 under 35 U.S.C. 101 as non-statutory because they are not tangibly embodied.

Without any concession regarding the substance of the rejection, which Applicant contends is incorrect, the Specification has been amended to remove reference to a carrier wave or other propagation medium.

It is submitted that the amendment fully responds to the rejection, and that the rejection should now be removed.

Claim Rejection under 35 U.S.C. §103

Chintalapati, et al. in view of Sugahara et al.

The Examiner rejected claims 1, 3, 4, 7-10, 12-14, 16-18, and 22-27 under 35 U.S.C. 103(a) as being unpatentable over U.S Patent No. 6,988,140 of Chintalapati, et al. ("*Chintalapati*") in view of U.S Patent No. 6,684,281 of Sugahara et al. ("*Sugahara*").

Claim 1, as amended herein, provides:

1. A method comprising:

initializing a computer system, the computer system including a first processor and a second processor;

designating the first processor to handle a polling function for a timer interrupt process for the computer system, a normal execution thread to be processed by the second processor;

setting a timer for a plurality of time intervals for the timer interrupt process;

calling a polling function at the end of each of the plurality of time intervals, the polling function being performed by the first processor, the polling function to determine if any special events have occurred; and

if the polling function results in a positive result, processing the results of the polling function with the second processor.

Thus, claim 1 initializing a computer system, with the computer system including a first processor and a second processor. In this process, the first processor is designated to handle a polling function for a timer interrupt process for the computer system, with a normal execution thread to be processed by the second processor. A timer is set for a plurality of time intervals for the timer interrupt process, and a polling function is called at the end of each of the plurality of time intervals, the polling function being performed by the first processor, the polling function to determine if any special events have occurred. If the polling function results in a positive result, the results of the polling function are processed with the second processor.

Chintalapati describes a mechanism for servicing connections by disassociating processing resources from idle connections. In addition to any other differences, *Chintalapati* does not suggest the use of a first process to perform a polling function and second processor to provide normal execution thread processing. Rather, the reference provides a processing resource, which is logical entity used by the server to service connection (*Chintalapati*, col. 6, lines 45-49), and a poll manager that receives idle connections from worker threads and passes active connections to a work queue

(*Chintalapati*, col. 6, lines 63-67). The concern addressed by the reference regards a recognition of the fact that there are times when a connection is idle and thus does not require servicing by the processing resource. (*Chintalapati*, col. 4, lines 52-60) It is respectfully submitted that the reference is not related to the processing of interrupts. In fact, the word "interrupt" does not even appear in the reference – there is no discussion of interrupt processing in any fashion. Rather, the reference is concerned with a different issue, which is avoiding the servicing of idle connections.

The Office Action states the following:

> Chintalapati does not explicitly teach the second processor. However, Sugahara teaches the second processor (the processor receiving the interrupt message ... by reading the interrupt message, col 1, ln 38-48).

It is respectfully submitted that *Sugahara* is not relevant to the element suggested in the Office Action, and in fact relates to interrupts sent between processors of different devices. *Sugahara* regards a process that is intended to provide for fast delivery of an interrupt message over a computer network (not efficient processing of interrupts for a computer system). It is respectfully submitted that this reference does not provide for a first processor operating with a second processor in a computer system, as described in claim 1. Rather, this reference provides a very different scenario, in which a first processor coupled to a computer network sends an interrupt message to a second processor coupled to the computer network.

The subject matter discussed in *Sugahara* is illustrated in Figures 1 and 2 of the reference. Figure 1 illustrates multiple devices 110A-110H that are attached to various PCI buses 120A-120C, with the buses being connected to a network router 103 via PCI

network adapters 130A-130C. More specifically, Figure 2 illustrates the specific issue, which regards a first processor (processor 210A) contained in a first device (device 110A) and a second processor (processor 210B) contained in a second device (device 110B, which is incorrectly denoted as 101B in Figure 2). The processor 210A is connected via a processor bus 220A to system memory 240A and a bridge (processor to PCI bridge 225A). The device 110A is connected to a PCI bus 120 A, which in turn is attached to a PCI network adapter 130A, which is connected to the network 103. Similarly, processor 210B is connected via a processor bus 220B to system memory 240B and a bridge (processor to PCI bridge 225B). The device 110A is connected to a PCI bus 120B, which in turn is attached to a PCI network adapter 130B, which is connected to the network 103. The interrupt process discussed in *Sugahara* regards this network structure.

For example, Figure 5 of *Sugahara* is a block diagram showing the path of an interrupt through logical components comprising the PCI network adaptors. However, as shown in Figure 5, the interrupt path at issue is from processor 210A of device 110A across PCI bus 120A, through the components of PCI network adaptor 130A, through the network router, across PCI bus 120B (incorrectly labeled 130B in Figure 5), through the components of PCI network adaptor 130B, to a circular buffer 141B of system memory 140B, which is a component of device 110B. This is the path taken by an interrupt message sent by processor 210A to processor 210B. (*Sugahara*, col. 7, lines 51-55) The manner in which this interprocessor interrupt is handled may be seen in part in Figure 3B, which illustrates how a PCI written to a "doorbell address" is transformed into an interrupt message. As shown, a normal write on PCI bus 120A goes to a doorbell space

341B of the PCI bu3 120 address space 300. This space is mapped to a doorbell space 382 of the PCI bus 120B address space 380.

Thus, *Sugahara* provides a process for interrupts between processors of different devices, rather than containing any teaching regarding the operations of a first processor of a computer system to handle a polling function and a second processor of the computer system to provided normal thread processing system. The process taught in the reference has no relation to the relevant limitations of claim 1, and thus neither of the cited references teaches or suggests these claim limitations.

It is submitted that the arguments provided above with regard to claim 1 also apply to independent claims 8, 14, and 22, and such claims are also allowable. The remaining rejected claims are dependent claims, which, in addition to other differences with the cited references, are allowable as being dependent on the allowable base claims.

With regard to claim 13, the Office Action indicates that Figure 2 of *Sugahara* teaches that a first processor and a second processor are logical processors in a single physical processor. However, Figure 2 does not contain any indication of such logical processors. The *Sugahara* reference does not contain any mention of logical processors, with any uses of the word "logical" regarding different concepts (such as in reference to logical components or logical partitions). Applicant requests clarification of this rejection.

Claim Rejection under 35 U.S.C. §103

Chintalapati, et al. in view of Sugahara et al. and further view of Booth

The Examiner rejected claims 2 and 11 under 35 U.S.C. 103(a) as being unpatentable over *Chintalapati* in view of *Sugahara* and further in view of U.S. Patent No. 6,065,073 of Booth (*"Booth"*).

The rejected claims are dependent claims, and are allowable as being dependent on the allowable base claims.

It is further noted that *Booth*, while cited for other purposes, does not appear to teach or suggest the claim limitations that are shown to be missing from *Chintalapati* and *Sugahara*. Thus, the references, taken separately or in any combination, do not teach or suggest all of the claim limitations. *Booth* specifically regards an auto-polling unit for interrupt generation in a network interface device, which regards auto-polling a status register within a physical layer to a local area network.

Claim Rejection under 35 U.S.C. §103

Chintalapati, et al. in view of Sugahara et al. and further view of Karnik et al.

The Examiner rejected claims 5 and 15 under 35 U.S.C. 103(a) as being unpatentable over *Chintalapati* in view of *Sugahara* and further view of U.S. Patent No. 5,724,527 of Karnik et al. (*"Karnik"*).

The rejected claims are dependent claims, and are allowable as being dependent on the allowable base claims.

It is further noted that *Karnik*, while cited for other purposes, does not appear to teach or suggest the claim limitations that are shown to be missing from *Chintalapati* and *Sugahara*. Thus, the references, taken separately or in any combination, do not teach or

suggest all of the claim limitations. *Karnik* relates to a boot strap mechanism for a multiprocessor system.

Claim Rejection under 35 U.S.C. §103

Chintalapati, et al. in view of Sugahara et al. and further view of Yamamoto

The Examiner rejected claim 6 under 35 U.S.C. 103(a) as being unpatentable over *Chintalapati* in view of *Sugahara* and further view of Japan Patent No. 405252374A of Yamamoto (*"Yamamoto"*).

The rejected claim is a dependent claim, and is allowable as being dependent on the allowable base claim.

It is further noted that *Yamamoto*, while cited for other purposes, does not appear to teach or suggest the claim limitations that are shown to be missing from *Chintalapati* and *Sugahara*. Thus, the references, taken separately or in any combination, do not teach or suggest all of the claim limitations.

Claim Rejection under 35 U.S.C. §103

Chintalapati, et al. in view of Sugahara et al. and further view of Yang et al.

The Examiner rejected claim 19 under 35 U.S.C. 103(a) as being unpatentable over *Chintalapati* in view of *Sugahara* and in further view of U.S. Patent No. 7,003,610 of Yang et al. (*"Yang"*).

The rejected claim is a dependent claim, and is allowable as being dependent on the allowable base claim.

It is further noted that *Yang*, while cited for other purposes, does not appear to teach or suggest the claim limitations that are shown to be missing from *Chintalapati* and *Sugahara*. Thus, the references, taken separately or in any combination, do not teach or

suggest all of the claim limitations. *Yang* relates to handling shared resource writes arriving via non-maskable interrupts in a single thread non-mission system.

Claim Rejection under 35 U.S.C. §103

Chintalapati, et al. in view of Sugahara et al. and further view of Hokenek et al.

The Examiner rejected claim 20 and 21 under 35 U.S.C. 103(a) as being unpatentable over *Chintalapati* in view of *Sugahara* and further in view of U.S. Patent No. 6,971,103 of Hokenek et al. (*"Hokenek"*).

The rejected claims are dependent claims, and are allowable as being dependent on the allowable base claims.

It is further noted that *Hokenek*, while cited for other purposes, does not appear to teach or suggest the claim limitations that are shown to be missing from *Chintalapati* and *Sugahara*. Thus, the references, taken separately or in any combination, do not teach or suggest all of the claim limitations. *Hokenek* relates to inter-thread communications using a shared interrupt register, with a multithreaded processor including an interrupt controller for processing a cross-thread interrupt directed from a requesting thread to a destination thread.

Conclusion

Applicant respectfully submits that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the claims as amended be allowed.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (503) 439-8778 if there remains any issue with allowance of the case.

Request for an Extension of Time if Needed

The Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) if one is needed. Please charge any fee to our Deposit Account No. 02-2666.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 10/15/07

Mark C. Van Ness
Reg. No. 39,865

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(503) 439-8778